NSD2621X

Half-bridge GaN Driver

Datasheet (EN) 0.3

Product Overview

NSD2621X is an integrated half-bridge gate driver which is designed for GaN transistors.

The driver operates with a wide supply voltage from 10V to 18V, while internal regulator could offer stable driver voltage to keep GaN transistors safe.

The undervoltage lock-out (UVLO) protection feature is provided in low side and high side drivers to prevent the GaN transistors from operating in low efficiency or dangerous conditions

The programmable dead-time control function has been provided.

The device operates in the industrial temperature range, -40°C to 125°C, and is available in a compact 4.0 x 4.0 mm QFN package.

Key Features

- 700V Half-bridge Gate Drivers
- Integrated High-side and Low-side Output Regulators
- UVLO protection on low side and high side
- Source Current: 2A/Sink Current: 4A
- Propagation Delay: 30ns TYP
- Short switching delay and mismatch
- Programmable Deadtime
- Allowable SW slew rate: 150V/ns
- Operating Temperature: -40~125°C

Applications

- Driving GaN power transistors
- Half-bridge, full-bridge, active flyback or forward, LLC DC-DC converter
- PFC and AC-DC converter

Device Information

Part Number	Package	Body Size
NSD2621A-DQAGR	QFN15	4.0 mm x 4.0 mm
NSD2621B-DQAGR	QFN15	4.0 mm x 4.0 mm
NSD2621C-DQAGR	QFN15	4.0 mm x 4.0 mm

Functional Block Diagram

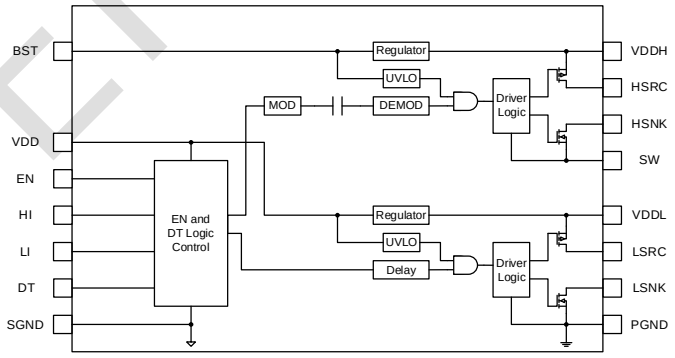

Figure 0.1 NSD2621X Block Diagram

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1. Pin Configuration and Functions

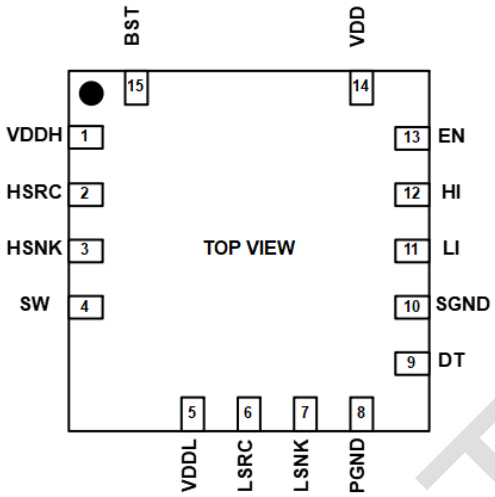


Figure 1.1 Pin Configuration

Table 1.1 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	VDDH	High-side voltage regulator output. A ceramic capacitor of not less than 100nF must be connected between VDDH and SW.
2	HSRC	High-side driver sourcing output
3	HSNK	High-side driver sinking output
4	SW	High-side driver reference (Switching node)
5	VDDL	Low-side voltage regulator output. A ceramic capacitor of not less than 100nF must be connected between VDDL and PGND.
6	LSRC	Low-side driver sourcing output
7	LSNK	Low-side driver sinking output
8	PGND	Low-side driver reference (Power ground)
9	DT	Dead-time adjustment
10	SGND	Signal ground
11	LI	Low-side driver logic input
12	HI	High-side driver logic input
13	EN	Dual drivers enabling logic input
14	VDD	Power supply for logic and low-side regulator
15	BST	Power supply for high-side regulator (Bootstrap voltage)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
High-side Common Mode Voltage	V_{SW}	-700	720	V
Driver Supply Voltage	VDD to SGND, BST to SW	-0.3	24	V
Regulator Output Voltage	VDDL to PGND, VDDH to SW	-0.3	7	V
Different Ground Voltage	SGND to PGND	-5	5	V
Input Signal Voltage	HI, LI, EN, DT to SGND	-0.3	V_{VDD}+0.3	V
	HI, LI, EN, DT to SGND, Transient for 50ns	-5	V_{VDD}+0.3	V
Driver Output Voltage	LSRC/LSNK to PGND, HSRC/HSNK to SW	-0.3	V_{VDDL}+0.3, V_{VDDH}+0.3	V
	LSRC/LSNK to PGND, HSRC/HSNK to SW, Transient for 50ns	-2	7	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-55	150	°C
Electrostatic Discharge	HBM (all pins)	-3000	3000	V
	CDM	-1000	1000	V

3. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
High-side Common Mode Voltage	V_{SW}	0	650	V
Driver Supply Voltage	VDD to SGND, BST to SW	10	18	V
Driver Output Voltage	LSRC/LSNK to PGND, HSRC/HSNK to SW	0	V_{VDDL}, V_{VDDH}	V
Input Signal Voltage	HI, LI, EN to SGND	0	V_{VDD}	V
Junction Temperature	T_J	-40	130	°C
Ambient Temperature	T_a	-40	125	°C

4. Thermal Information

Parameters	Symbol	Value	Unit
Junction-to-ambient thermal resistance[1)]	θ_{JA}	75.8	°C/W
Junction-to-case(top) thermal resistance[1)]	$\theta_{JC\ (top)}$	19	°C/W
Junction-to-board thermal resistance[1)]	θ_{JB}	65.6	°C/W
Junction-to-top characterization parameter[1)]	Ψ_{JT}	55.5	°C/W

Junction-to-board characterization parameter[1)]	Ψ_{JB}	49.7	°C/W

1) High Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.

5. Specifications

5.1. Electric Characteristics

VDD = 12V, Ta = -40°C to 125°C. Unless otherwise noted, Typical values are at Tj = 25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Driver Power Supply						
VDD Quiescent Current	I_{VDDQ}		0.42		mA	HI = LI = 0V
VDD Operating Current	I_{VDDO}		2.6		mA	HV = SW = 0V, BST = 12V, f = 500kHz， C_{load} = 330pF
BST Quiescent Current	I_{BSTQ}		0.55		mA	HI = LI = 0V
BST Operating Current			2.7		mA	HV =SW = 0V, BST = 12V, f = 500kHz， C_{load} = 330pF
VDD UVLO Rising Threshold	V_{VDD_ON}	8.1	8.4	8.8	V	
VDD UVLO Falling Threshold	V_{VDD_OFF}	7.5	7.8	8.1	V	
VDD UVLO Hysteresis	V_{VDD_HYS}	0.4	0.6	/	V	
BST UVLO Rising Threshold	V_{BST_ON}-V_{SW}	8.1	8.4	8.8	V	
BST UVLO Falling Threshold	V_{BST_OFF}-V_{SW}	7.5	7.8	8.1	V	
BST UVLO Hysteresis	V_{BST_HYS}	0.4	0.6	/	V	
Input Logic						
Input Pin Pull-down Resistance	R_{HI_PD}, R_{LI_PD}		200		kΩ	HI = LI = 3V
Enable Pin Pull-down Resistance	R_{EN_PD}		200		kΩ	EN = 3V
Input Pin High Logic Bias Current	I_{HI_H}, I_{LI_H}		20		μA	HI = LI = 5V
Enable Pin High Logic Bias Current	I_{EN_H}		20		μA	EN = 5V
Logic High Input Threshold	V_{HI_H}, V_{LI_H}	1.7	2.1	2.5	V	
Logic Low Input Threshold	V_{HI_L}, V_{LI_L}	0.9	1.2	1.5	V	
Input Hysteresis	V_{HI_HYS}, V_{LI_HYS}	0.7	0.9		V	
Logic High Input Threshold	V_{EN_H}	1.7	2.1	2.5	V	
Logic Low Input Threshold	V_{EN_L}	0.9	1.3	1.5	V	
Input Hysteresis	V_{EN_HYS}		0.8		V	
Driver Output Characteristic						

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Regulator Output Voltage	V_{VDDL}, V_{VDDH}-V_{SW}	5.7	6	6.3	V	C_{VDDL} = 100nF, $C_{VDDH-SW}$ = 100nF, NSD2621A
		5	5.4	5.8	V	C_{VDDL} = 100nF, $C_{VDDH-SW}$ = 100nF, NSD2621B
		4.6	5	5.3	V	C_{VDDL} = 100nF, $C_{VDDH-SW}$ = 100nF, NSD2621C
Regulator UVLO Rising Threshold	V_{VDDH_ON}, V_{VDDL_ON}	4.2	4.4	4.6	V	
Regulator UVLO Falling Threshold	V_{VDDH_OFF}, V_{VDDL_OFF}	3.9	4.1	4.3	V	
Regulator UVLO Hysteresis	V_{VDDH_HYS}, V_{VDDL_HYS}		0.3		V	
High−level output voltage, V_{VDDH}−V_{HSRC} or V_{VDDL}−V_{LSRC}	V_{OH}		16		mV	I_SRC = 10 mA
Low−level output voltage, V_{HSNK}−V_{SW} or V_{LSNK} −PGND	V_{OL}		8		mV	I_SNK = 10 mA
Output Peak Source Current	I_{LSRC_PK}, I_{HSRC_PK}		2		A	
Output Peak Sink Current	I_{LSNK_PK}, I_{HSNK_PK}		4		A	

5.2. Dynamic Characteristics

VDD=12V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at Ta=25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Input Pulse Width	t_{PWmin}			20	ns	
Output Rising Time	t_{LSRC}/t_{HSRC}		5		ns	C_{load} = 330pF
Output Falling Time	t_{LSNK}/t_{HSNK}		3		ns	C_{load} = 330pF
Turn-on Propagation Delay Time	$t_{PD(on)}$		30	60	ns	
Turn-off Propagation Delay Time	$t_{PD(off)}$		30	60	ns	
Propagation Delay Match	t_{PDM}			10	ns	
Pulse Width Distortion	t_{PWD}			10	ns	
VDD or BST Power-up Delay Time[1)]	t_{PUD}		22		µs	First time power-up from V_{POR}
VDDL or VDDH Rising Time[1)]	t_{VDDL_R}/ t_{VDDH_R}		15		µs	C_{VDDL}= 100nF, $C_{VDDH-SW}$ = 100nF
Programmed Deadtime	t_{DT_Min}		20		ns	R_{DT} <= 20kΩ or R_{DT}>354kΩ, C_{DT} = 1nF
	t_{DT_Linear}		R_{DT}(kΩ)		ns	20kΩ< R_{DT} <= 100kΩ, C_{DT} = 1nF
	t_{DT_Max}		100		ns	100kΩ<R_{DT} <= 354kΩ, C_{DT} = 1nF

1) See detail in Chapter 6.1.

5.3. Typical Performance Characteristics

T_J = 25°C, unless otherwise noted.

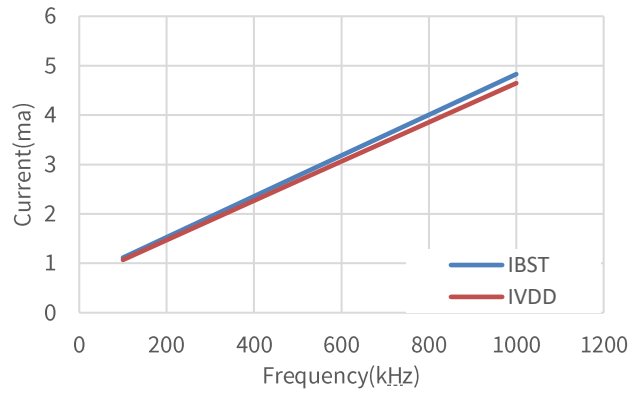


Figure 5.1 Operating Current (I_VDD, I_BST) vs. Frequency (VDD = VBST=12 V, SW = PGND, 330pF load)

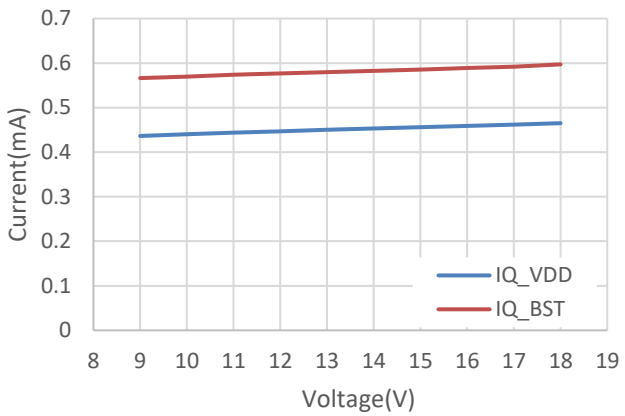


Figure 5.2 Quiescent Current (IQ_VDD, IQ_BST) vs. Voltage

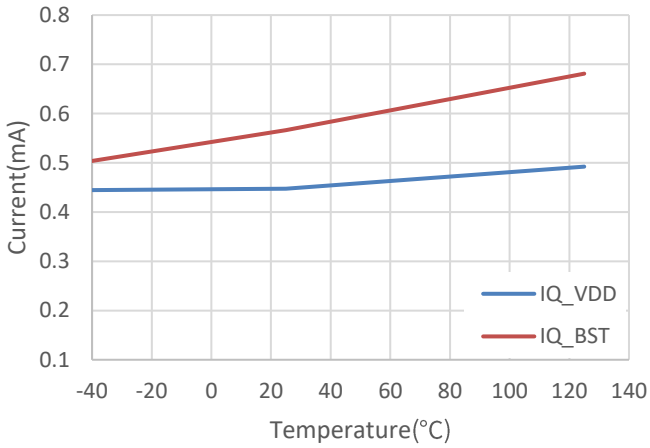


Figure 5.3 Quiescent Current (IQ_VDD, IQ_BST) vs. Temperature

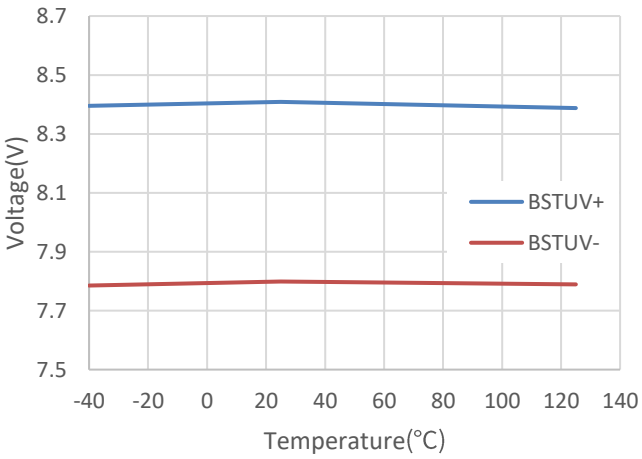


Figure 5.4 BST UVLO vs. Temperature

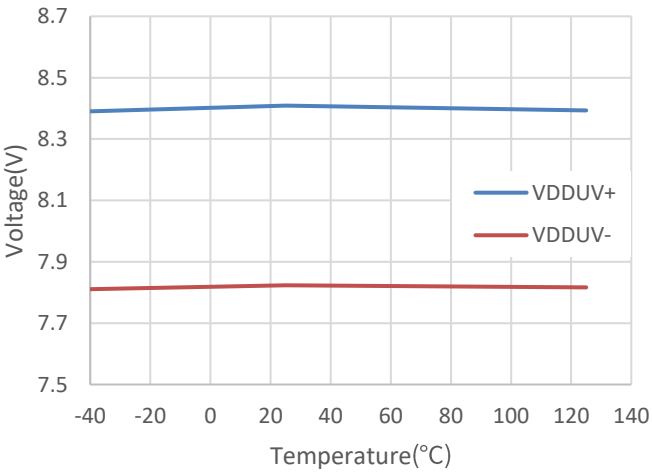


Figure 5.5 VDD UVLO vs. Temperature

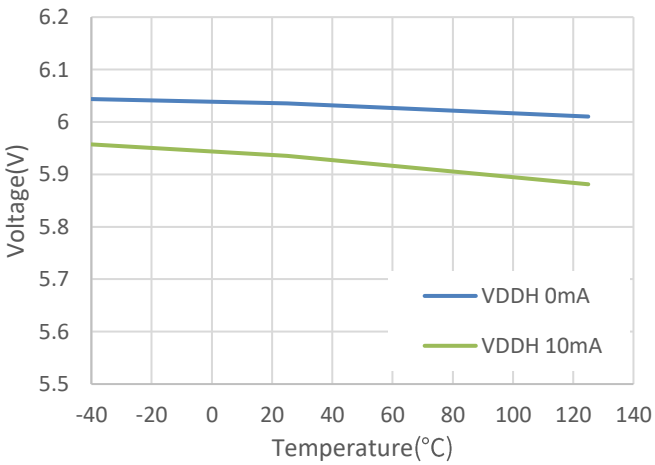


Figure 5.6 VDDH Output Voltage vs. Temperature

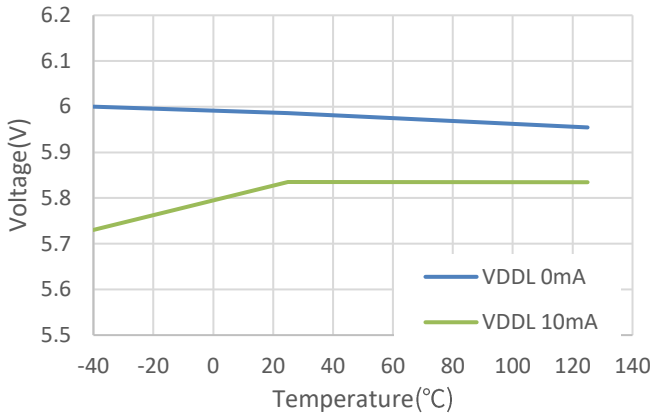


Figure 5.7 VDDL Output Voltage vs. Temperature

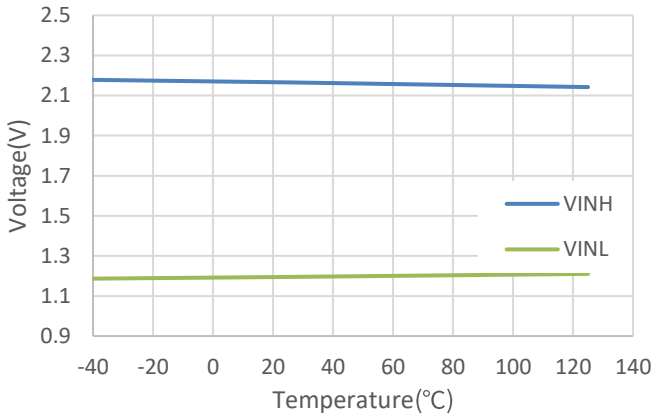


Figure 5.8 Input Logic (HI, LI) Threshold vs. Temperature

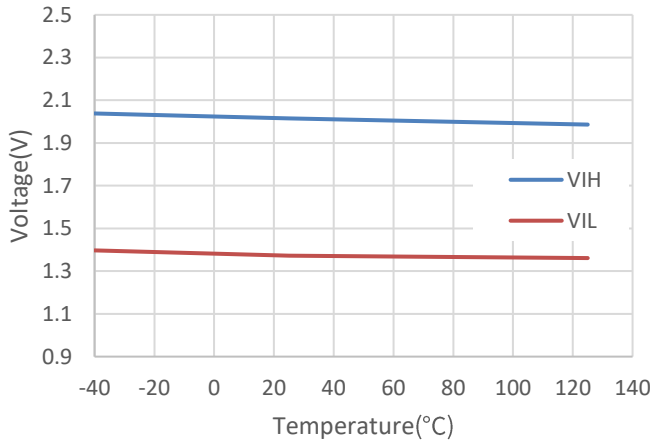


Figure 5.9 Input Logic (EN) Threshold vs. Temperature

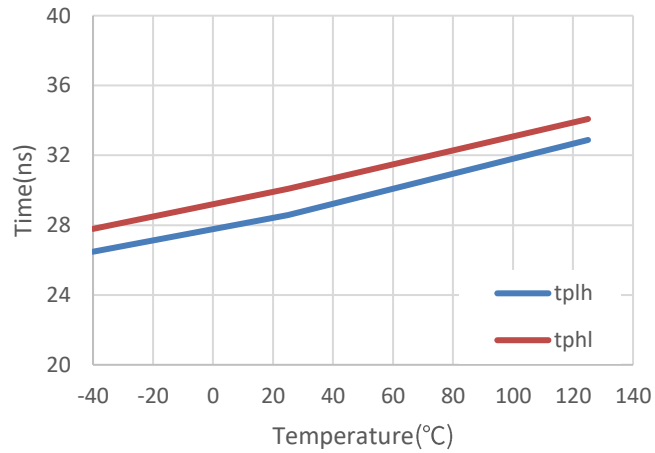


Figure 5.10 LI to LSRC & LSNK Propagation Delay vs. Temperature

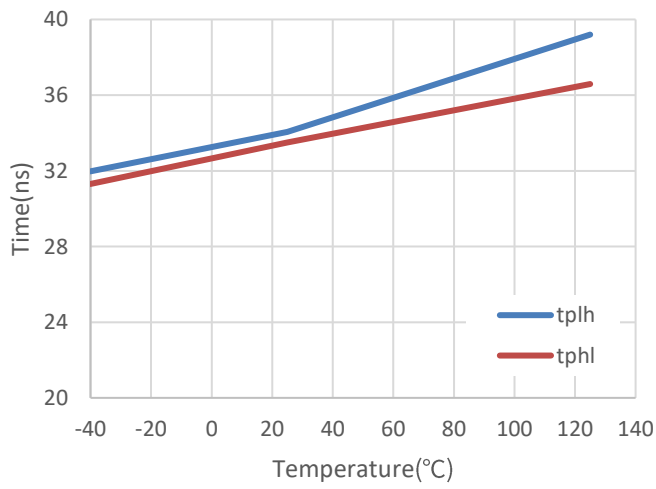


Figure 5.11 HI to HSRC & HSNK Propagation Delay vs. Temperature

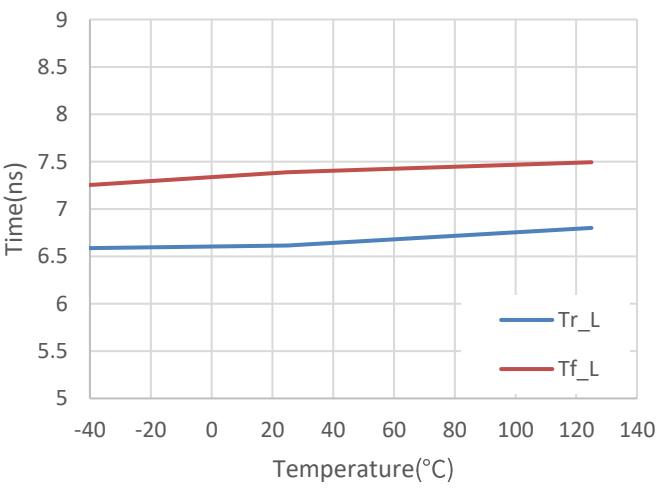


Figure 5.12 LSRC Rise Time and LSNK Fall Time vs. Temperature

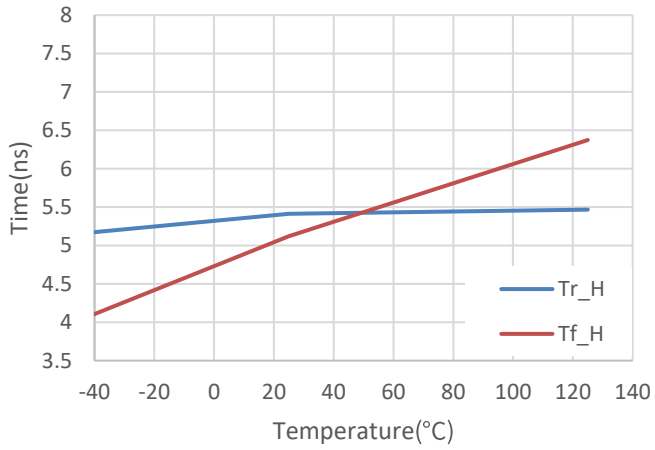


Figure 5.13 HSRC Rise Time & HSNK Fall Time vs. Temperature

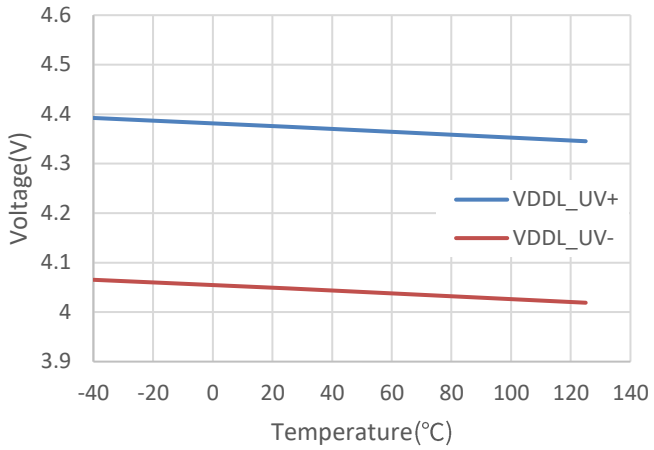


Figure 5.14 VDDL UVLO vs. Temperature

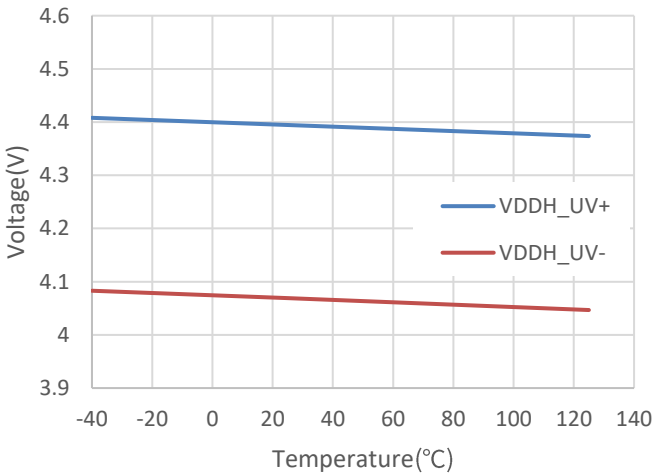


Figure 5.15 VDDH UVLO vs. Temperature

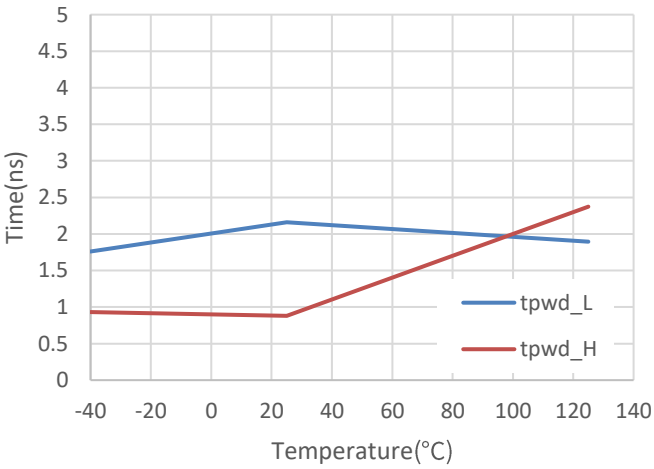


Figure 5.16 Pulse Width Distortion vs. Temperature

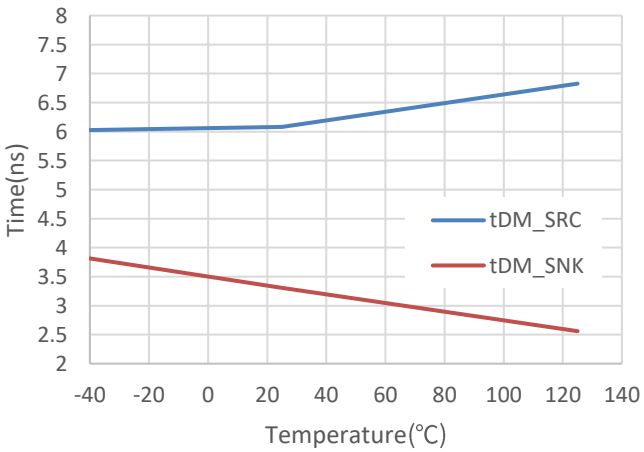


Figure 5.17 Propagation Delay Matching (HI to HO, LI to LO) vs. Temperature

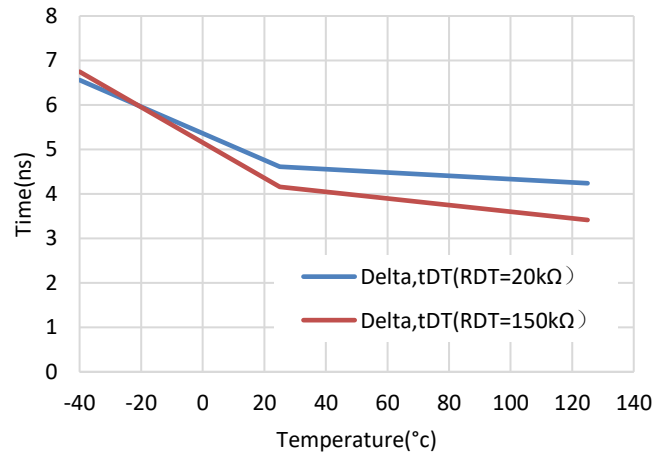


Figure 5.18 Dead-time Mismatch vs. Temperature

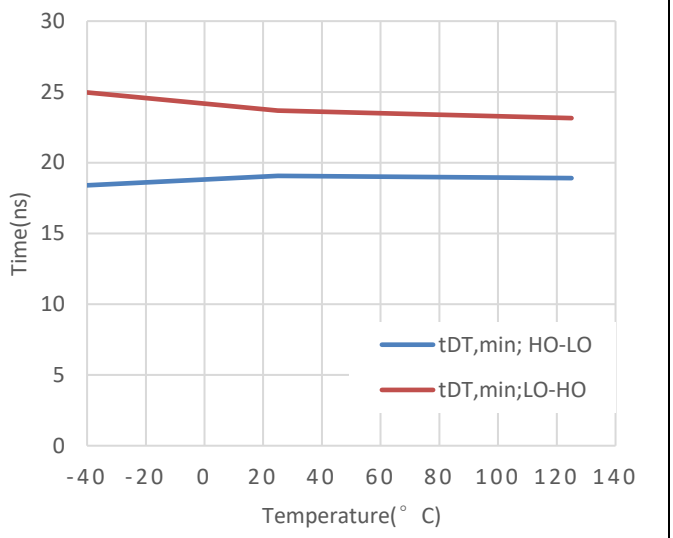


Figure 5.19 Minimum Dead−time (RDT = 20kΩ) vs. Temperature

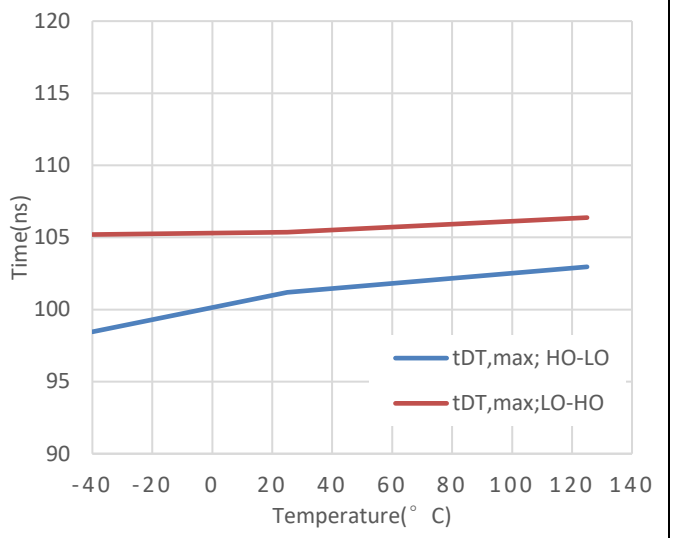


Figure 5.20 Maximum Dead−time (RDT = 150kΩ) vs. Temperature

5.4. Parameter Measurement Information

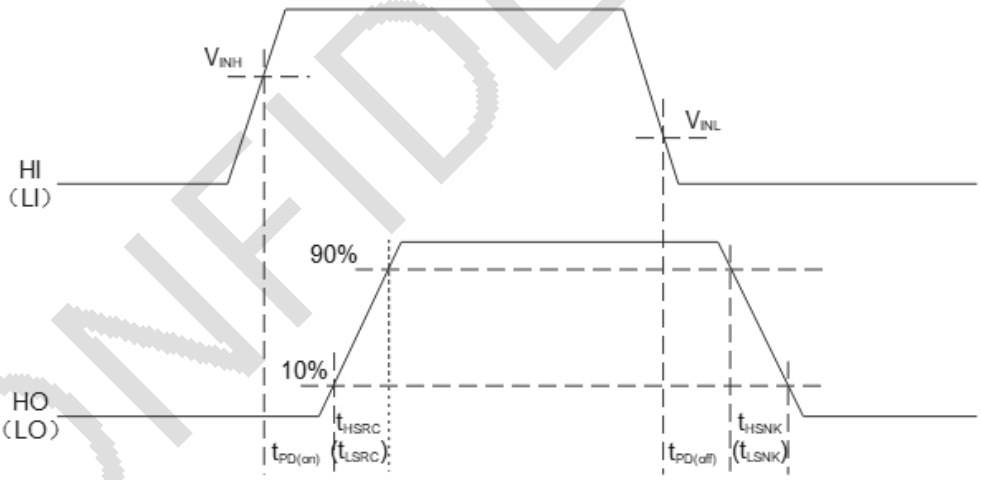


Figure 5.21 Switching Time Waveform

6. Function Description

6.1. Under Voltage Lock Out (UVLO)

The NSD2621X has internal under voltage lock out (UVLO) protections on low side and high side power supply blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDD or BST is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins.

The 0.5V hysteresis (V_{VDD_HYS}) on VDD and BOOT ULVO protections are provided prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup. The recovery propagation time of V_{VDDL} is about 1us when V_{VDD} voltage fall from more than V_{VDD_ON} to some value between V_{VDD_OFF} and V_{VDD_POR} and then raise to more than V_{VDD_ON}.

A not less than 100nF ceramic capacitor must be used on VDDL and VDDH to normally operate.

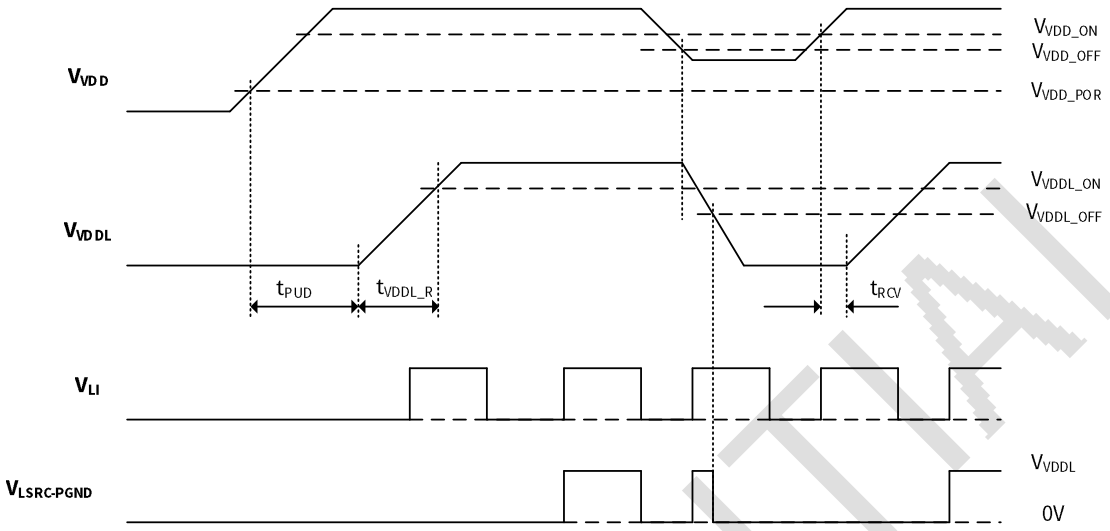


Figure. 6.1 UVLO Diagram

6.2. Input and Output Logic

The NSD2621X is a half-bridge gate driver with dead-time control. The EN pin should be logic high to keep the driver operating normally.

Table 6.1 Output status vs. Input and Power status

Input Pins			Output Pins		NOTE
EN	HI	LI	HSRC/HSNK	LSRC/LSNK	
L or O	X	X	L	L	
H	L	L	L	L	
H	L	H	L	H	Driver's outputs turn on after the deadtime expires.
H	H	L	H	L	
H	H	H	L	L	The input signal is later than VDD power up.

1) H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

6.3. Programmable Deadtime (DT pin)

The NSD2621X has a programmable deadtime control function by placing a resistor, R_{DT}, between the DT pin and SGND. There are three statuses of deadtime program.

1) While R_{DT} is lower than 20kΩ or higher than 354kΩ, the deadtime duration (t_{DT}) is set to 20ns.
2) While R_{DT} is in range of 20kΩ to 100kΩ, the t_{DT} can be determined from Equation 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 1 \times R_{DT} \quad (1)$$

3) While R_{DT} is in range of 100 kΩ to 354kΩ, the deadtime duration (t_{DT}) is set to 100ns.

The recommended value of R_{DT} is between from 1kΩ to 200kΩ. It is also recommended to parallel a ceramic capacitor, for example 1nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal's falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 6.2:

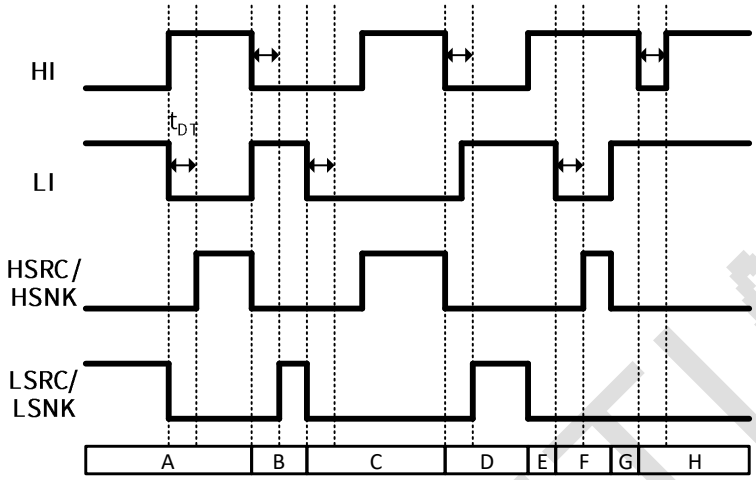


Figure. 6.2 Input and Gate Logic with the Programmed Deadtime

Condition	*Result*
A: HI goes high, and LI goes low.	LSRC/LSNK goes low immediately, then HSRC/HSNK goes high after the programmed deadtime which is assigned at LI goes low.
B: HI goes low, and LI goes high.	HSRC/HSNK goes low immediately, then LSRC/LSNK goes high after the programmed deadtime which is assigned at HI goes low.
C: LI goes low, then HI goes high after deadtime.	LSRC/LSNK goes low immediately, then HSRC/HSNK goes high immediately when HI goes high.
D: HI goes low, then LI goes high before deadtime.	HSRC/HSNK goes low immediately, then LSRC/LSNK goes high after deadtime
E: HI goes high, LI is still high.	LSRC/LSNK goes low immediately, and HSRC/HSNK keeps low.
F: HI is still high, LI goes low.	HSRC/HSNK goes high after deadtime while LI is low, and LSRC/LSNK keeps low.
G: HI is still high, LI goes high after deadtime	HSRC/HSNK goes low immediately, and LSRC/LSNK keeps low.
H: HI goes low then goes high before deadtime while LI is still high.	HSRC/HSNK keeps low and LSRC/LSNK keeps low because deadtime control.

7. Application Note

7.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the NSD2621.

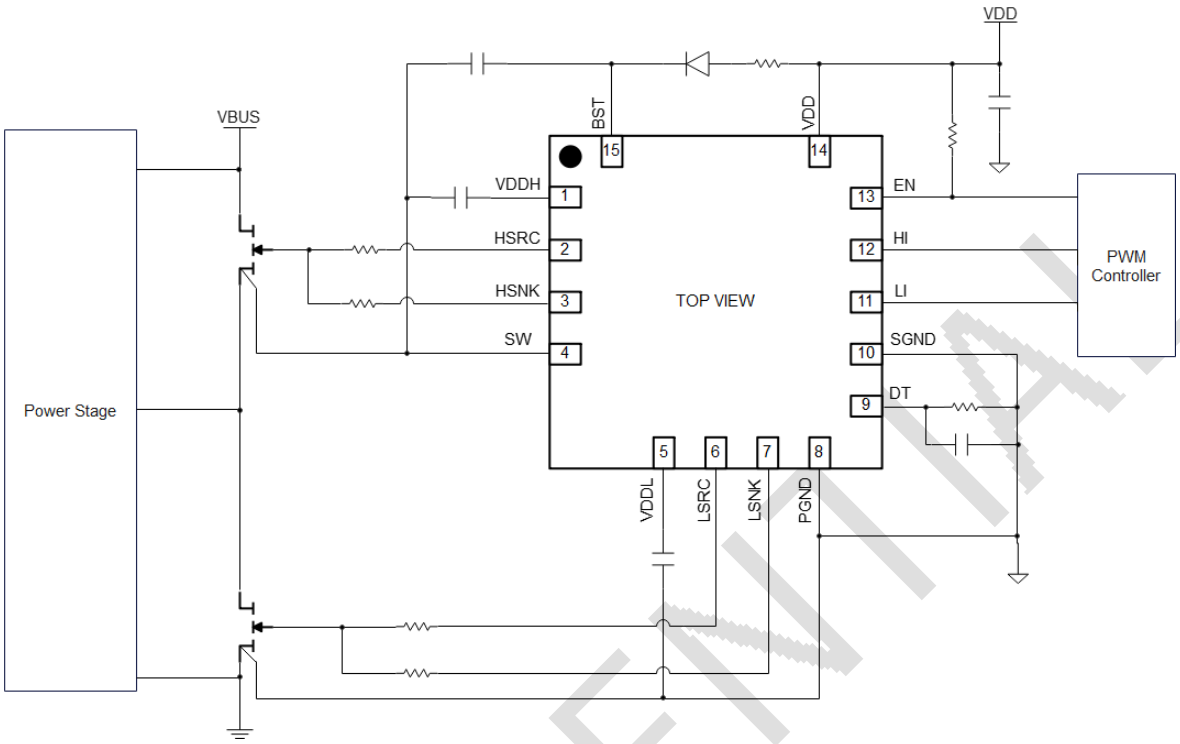


Figure. 7.1 Simplified Half-Bridge Application Schematic

7.2. Layout Recommendations

PCB layout is important to get optimal performance. Some of the layout guidelines to be followed are listed below:

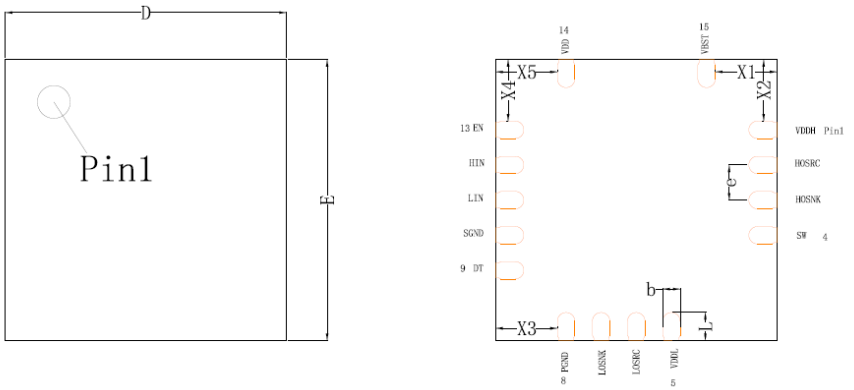
1) The bypass capacitors connected on VDD, VDDH, VDDL, EN, DT and BST should be placed as close to their respective pins as possible.
2) A not less than 100nF MLCC capacitor should be placed between VDDL and PGND.
3) A not less than 100nF MLCC capacitor should be placed between VDDH and SW.
4) High frequency switching current that charges and discharges the gate and drain of GaN FETs, that causes EMI and ringing issues. The lengths of gate drive loop should be short to minimum the parasitic inductance and ringing affection.
5) The source and sink gate drive resistors should be placed as close to the GaN FETs as possible.

8. Package information

Package Top View

Package Bottom View

Package Side View



SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.007	0.012	0.017
D	3.900	4.000	4.100
E	3.900	4.000	4.100
e	0.450	0.500	0.550
b	0.200	0.250	0.300
L	0.350	0.400	0.450
X1	0.825	0.875	0.925
X2	0.825	0.875	0.925
X3	0.825	0.875	0.925
X4	0.825	0.875	0.925
X5	0.825	0.875	0.925

Figure. 8.1 Package Shape and Dimension

9. Ordering Information

Part No.	*Temperature*	*Auto-motive*	*Package Type*	*Package Drawing*	*MSL*	*SPQ*
NSD2621A-DQAGR	-40 to 125° C	NO	QFN	QFN	3	2500
NSD2621B-DQAGR	-40 to 125° C	NO	QFN	QFN	3	2500
NSD2621C-DQAGR	-40 to 125° C	NO	QFN	QFN	3	2500

10. Tape and Reel Information

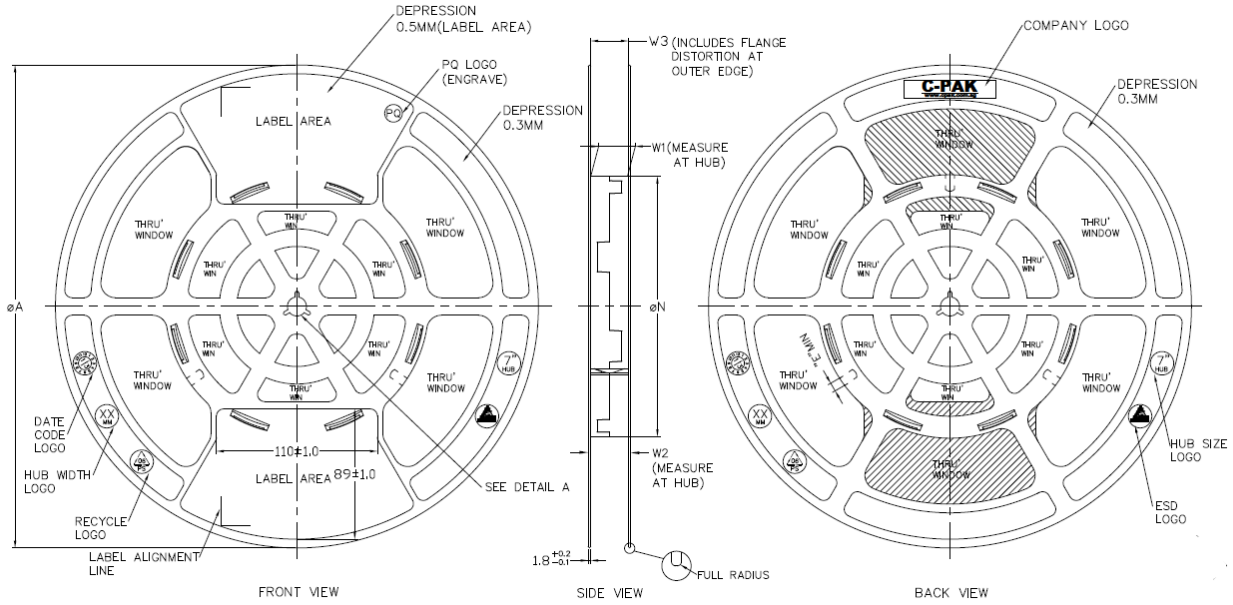


Figure. 10.1 Tape Information

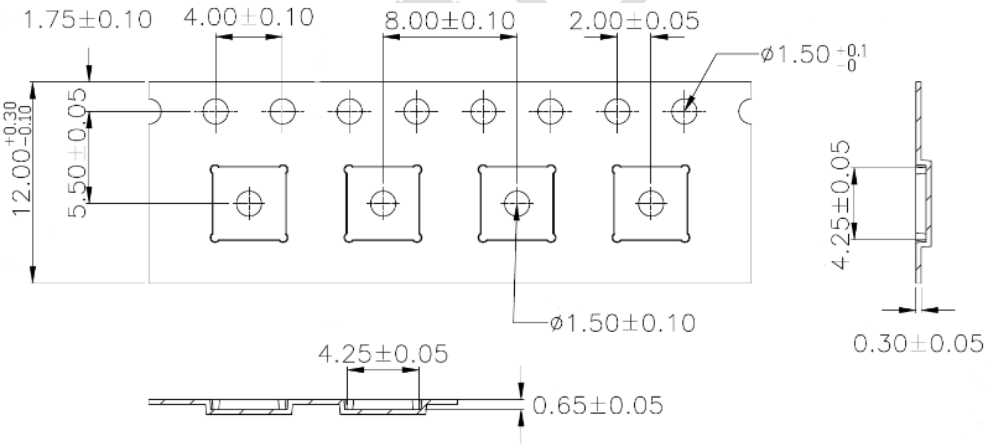


Figure. 10.2 Reel Information

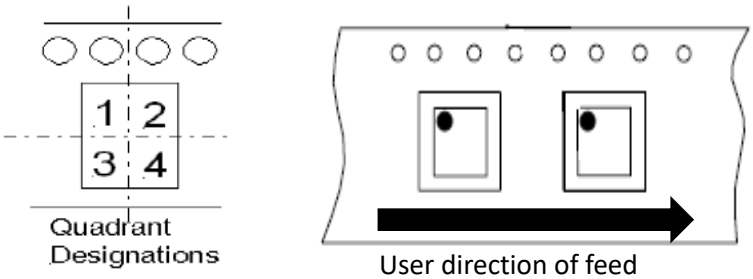


Figure. 10.3 Quadrant Designation for Pin1 Orientation in Tape

11. Revision History

Revision	Description	Date
0.1	Initial internal version	2022/6/20
0.2	Update part number and product description information	2022/10/25
0.3	Update Package information	2023/05/08

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